

Pressure Sintering for Thermal Stack Assembly

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Abstract

Pressure sintering of silver powder is an alternative bonding and joining technology for high temperature applications. Especially large area soldering joins need to be substituted by a more reliable and better performing technique. Those layers are found between ceramic substrates (DBC) and the metallic base plate which are forming the so called thermal stack.

In this paper optimized thermal stacks are presented. The interconnection layer between DBCs and a copper base plate is produced by pressure sintering of silver powder. To achieve high temperature cycle capability it was necessary to increase the thickness of the silver layer from normally $10\mu\text{m}$ to about $100\mu\text{m}$. Different layer thicknesses and bonding forces are discussed. The thermal stack demonstrators are exposed to temperature cycles and reliability results are presented.

It will be shown, how thick silver sinter layers increase the reliability of thermal stacks in advanced applications. Thermal simulation results as well as results of thermal cycling tests will be presented and discussed.

1 Introduction

1.1 Power Modules

Power modules are usually consisting of those electronic elements which have considerably high power losses in terms of heat, like power transistors or diodes. These components are part of more extended electronic systems responsible for controlling speed and torque of electrical loads like motors. Standard printed circuit boards (epoxy or polyimide boards) are limited in their capability of draining heat from specific components [1].

Typical power modules are building a thermal stack consisting of multiple semiconductors (bare die) on top of a high power substrate (Direct Bonded Copper - DBC) which is assembled onto a copper heat sink (see Fig. 1).

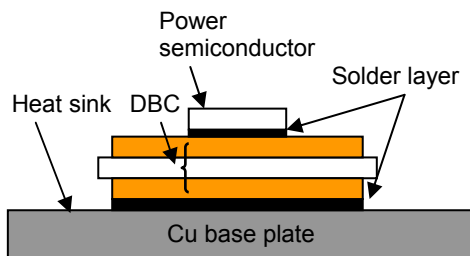


Fig. 1 Principle thermal stack with semiconductor, solder layers, DBC and heat sink

The standard assembly of bare dies, DBCs and heat sinks is a vacuum soldering process for void-free layers with lead-free solder alloys.

The use of pressure sintering for the principle assembly of substrates on base plates is already reported in [2]. Klaka did not report details of thicknesses and lifetime results, which is the content of this article.

1.2 Soldering – State of the Art of Bonding and Joining

Trends of higher integration and miniaturization of electronic components into electrical engines lead to increased operating temperatures. In some applications the ambient temperature already exceeds 150°C . Standard bonding and joining techniques use soft solders and adhesives to connect electrical components to substrates. Some components like power semiconductors even operate at more than 200°C due to power losses and high ambient temperatures. Higher peak operating temperatures result in higher temperature swings when systems are turned on and off.

It is well known that soft solders suffer from rapid degradation already above 120°C [3]. Temperature cycling and thermal mismatch between components, substrates and heatsinks during operation additionally lead to early cracks in the interconnecting layers [4].

With thicker solder joints the growing of the cracks can be reduced. Ultrasonic scans of a demonstrator with a DBC area of 23 x 18mm² soldered on a 2,5mm thick Cu base plate (35mm x 60mm) reveal the cracks in the solder joint. Figure 2 shows the crack propagation for a different number of temperature cycles (-40°C to +125°C, 30min dwell time) and two solder layer thicknesses (200µm and 400µm).

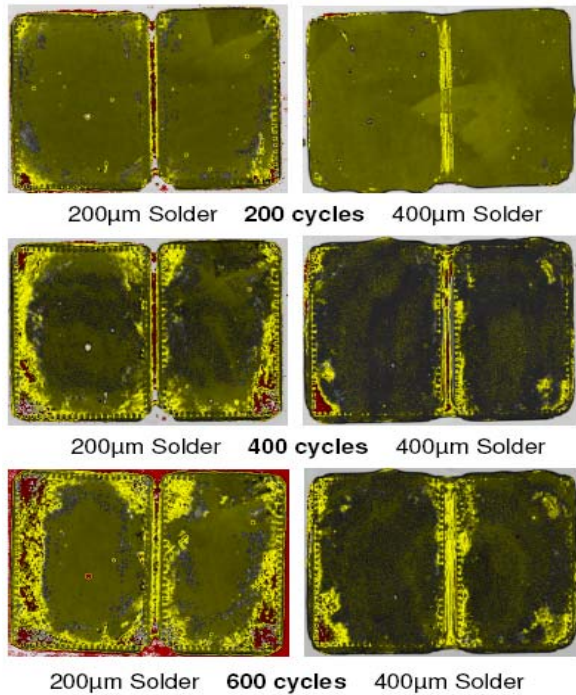


Fig. 2 Growing cracks, subject to solder thickness and number of temperature cycles (Ultrasonic imaging by Sonoscan[®], TU-Dresden). Dark areas are solid solder layers, light green or red areas are indicating cracks in the solder layers

Tab. 1 Standard thermal stack acc. to Fig.1 with thermal properties per layer and in total. Parameter: Substrate bonding **200 µm solder layer**

200µm SnAg3.5 - Simple Thermal Stack Analysis				
Layer thickness	Material selected	Theta	ΔT _{jc} due to this layer	Weighted effect of layer
mm		K/W	K	%
0,20	Silicon	0,021	2,1	6,9
0,08	Solder	0,026	2,6	8,4
0,30	Copper	0,011	1,1	3,5
0,40	AL ₂ O ₃ 96	0,158	15,8	52,0
0,30	Copper	0,007	0,7	2,3
0,40	Solder	0,031	3,1	10,2
2,50	Copper	0,050	5,0	16,6
Totals		0,304	30,4	100,0

As a result of thicker solder layers the thermal resistance of the module (R_{th}) increases. A simple thermal stack analysis reveals the different junction temperature rise for 100 Watts of dissi-

pated power (die size 8x8mm²) with SnAg3.5 solder (TC = 47 W/mK).

Table 1 and 2 compare two thermal stack arrangements which only differ in the thickness of the substrate solder layer. In both stacks this solder layer represents 10,2% (200µm solder) respectively 18,1% (400µm solder) of the ΔT_{jc} (resp. R_{th}). This clearly shows the importance of the layer material for the total R_{th} .

Tab. 2 Standard thermal stack acc. to Fig.1. with thermal properties per layer and in total. Parameter: Substrate bonding **400 µm solder layer**

400µm SnAg3.5 - Simple Thermal Stack Analysis				
Layer thickness	Material selected	Theta	ΔT _{ja} due to this layer	Weighted effect of layer
mm		K/W	K	%
0,20	Silicon	0,021	2,1	6,5
0,08	Solder	0,026	2,6	7,9
0,30	Copper	0,010	1,0	3,2
0,38	AL ₂ O ₃ 96	0,156	15,6	47,9
0,30	Copper	0,007	0,7	2,1
0,40	Solder	0,059	5,9	18,1
2,50	Copper	0,047	4,7	14,3
Totals		0,325	32,5	100,0

Additionally with increased solder layers the process stability decreases, because the DBC tends to tilt during the solder process. Tilted DBC substrates are root cause for early cracks in the solder layer due to the critical low thickness. Often specific and costly tools and processes are necessary to keep the substrate in place and in correct orientation during the soldering process.

2 Pressure Sintering

Pressure sintering of silver powder known as LTJT (Low Temperature Joining Technique) or NTV (German abbreviation for: Niedertemperatur-Verbindungstechnik) can be used to assemble power electronics modules.

2.1 LTJ Process

The basis for the bonding and joining process is powder made from idle materials like silver.

The silver flakes offer spontaneous sinter ability at a temperature of above 220°C. The pressure enhances the sinter ability tremendously due to the increased active contact area between the individual silver particles. To prevent the silvers from sintering at room temperature the silver flake is enriched with an organic additive. Decomposing of the organic coating around the silver flake takes place at a temperature of above 220°C under oxygen atmosphere. Heating above the decomposing temperature, higher pressing

and longer sinter processes support the sintering process of the LTJ silver flakes. The usual sintering process is carried out at 30 MPa of force, 250°C for 1 minute and results in a porosity of the sintered silver layer of about 15%. It is necessary to provide an oxide-free surface of the components to be joined for sufficient adhesion forces. A Ni diffusion barrier and Au finish provide sufficient oxide-free surfaces for further LTJ joining processes.

To apply the powder to the surface several layering techniques are usually applied: Spraying, screen or stencil printing and transferred preforms. These techniques differ in the cost of coating and in their risk of correct application in terms of homogenous thickness and the absence of agglomerations [5][6].

2.2 Hydraulic Press

The equipment used is a high precision 2-column press with a pneumohydraulic linear drive. The Institute of Mechatronics (University of Applied Sciences in Kiel) is equipped with different units up to 1000kN.

To perform the sinter task a 500kN press is used (see Fig.3). The bottom punch is equipped with a heating unit and the top punch has a rubber fill to assure uniform pressure for the joined elements.



Fig. 3 Pneumohydraulic high precision 2-column press (500kN) with an electrical heater in the bottom punch and parameter monitoring equipment.

The process is computer controlled and monitored for temperature, force and path lengths of compression.

2.3 Bond Strength Qualification

To determine the bond strength of the silver powder connection a peel test was performed [4].

First a silver stripe with a thickness of 100µm was joined to the DBC substrate (metallized with Ni/Au, see Fig. 4). Then the sample was attached to the sliding support and the free end of silver stripe was pulled up while the peeling force was measured. The sliding support assures a constant peeling angle during the test phase.

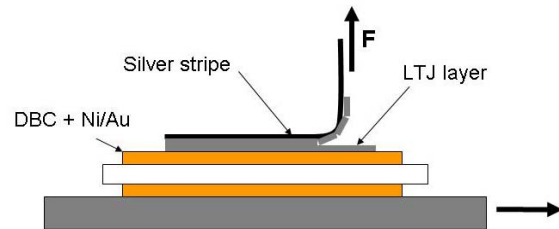


Fig. 4 Sliding peel-test with constant angle of the pulling force

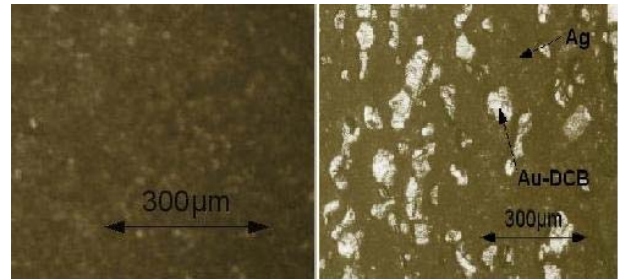


Fig. 5 Right: Optical microscope image of cohesion fracture on the DBC substrate with low pressure. Left: Adhesion and cohesion fracture on the DBC substrate with high pressure

Cohesion fracture within the silver layer is shown in Fig. 5. This fracture morphology indicates that the interfacial strength between the sintered Ag and Au metallization was higher than the strength of the sintered Ag layer. Left picture (after the peeling test): The surface of the DBC was covered with a layer of thin sintered silver. This type of crack is typical for high pressure and a sintering temperature over 220°C.

The typical peel force for this kind of fracture amounts to about 6 N/mm (force / stripe width). If the adhesion forces are lower or equal to the cohesion forces then the fracture path can be similar as shown in Fig. 5 (right picture). In this case the peel strength is usually lower than 6 N/mm. Numerous voids without sintered silver are to be seen on the peeled DBC surface.

High process temperature, high pressure and long process duration improve the diffusion bonding forces within the Ag sinter layer as well as the interface between the Ag and Au metallization.

3 Application

3.1 Motivation for Using Pressure Sintering of Silver

The results from advanced soldering processes reported above do not meet all of the industrial requirements. Thermal and mechanical properties still need optimization in terms of R_{th} and thermal cycle capability. Especially automotive applications, like electric power steering, hybrid electric traction, DC-DC-conversion require a relatively high thermal cycle capability. This means: Small CTE mismatch between substrate and heat sink respectively high shear strength of the bonding layer. A perfect design should also offer the lowest possible R_{th} (low R_{th} = low semiconductor area = inexpensive design).

With an assembly of DBC-substrates and heat sinks by a silver based pressure sintering process both requirements can be fulfilled. Table 3 is a thermal analysis of the stack with silver sintered layer instead of a solder layer. The contribution of the silver layer to thermal resistance drops down to 1,1% (resp. ΔT_{jc} drops to only

100µm Sintered Ag - Simple Thermal Stack Analysis				
Layer thickness	Material selected	Theta	ΔT_{jc} due to this layer	Weighted effect of layer
mm		K/W	K	%
0,20	Silicon	0,021	2,1	7,5
0,08	Solder	0,026	2,6	9,1
0,30	NiAu+Copper	0,011	1,1	3,8
0,40	AL ₂ O ₃ 96	0,161	16,1	57,2
0,30	Copper+NiAu	0,007	0,7	2,6
0,10	Sintered Ag	0,003	0,3	1,1
2,50	NiAu+Copper	0,052	5,2	18,7
Totals		0,281	28,1	100,0

28,1K)

Tab. 3 Standard thermal stack acc. to Fig.1. with thermal properties per layer and in total. Parameter: Substrate bonding 100 µm pressure sintered Ag layer. Note the small contribution of LTJ-Silver to the total ΔT_{jc}

3.2 Test Specimen

The test module is based on the automotive electric power steering module (see Fig. 6 and 7) with dimension explain in Chap.1.2. For comparison an aluminum base plate alternative to a copper plate was used.

The mechanical and thermal connections were realized by the LTJ-layer in the pressure sintering process. To find out the dependency between the LTJ-layer thickness and the module reliability three thicknesses were analyzed 25µm, 50µm and 100µm respectively.

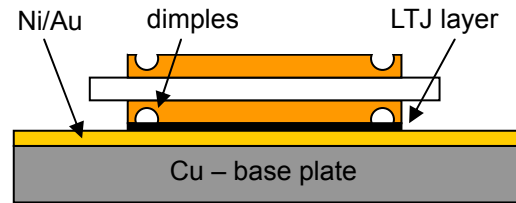


Fig. 6 Cross section of the test sample

To assure oxide free surface areas for the joining process a Ni/Au metallization was deposited for DBC substrate and base plate. The LTJ layer was applied by using the transfer/preform method.

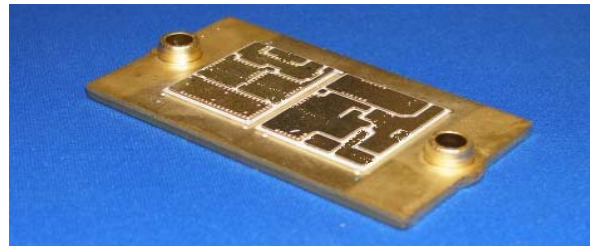


Fig. 7 Test sample. Copper base plate and DBC substrates with Ni/Au metallization

3.3 Test Conditions

The temperature cycling test (-40°C to +125°C, EN 60068-2-14) was applied to analyze the reliability of the test samples. Test samples were arranged in pairs and torqued together back to back in order to reproduce the final mounting the power modules to the heat sink. The temperature cycling test was performed periodically in two thermal chambers whereas the dwell time was 30 minutes. After 500, 1000 and 1500 cycles the temperature test was interrupted and the sintered layers were inspected. Two analysis methods were used to analyze the status of the joints. To detect the fracture within the sintered silver layer the ultrasonic microscope method was used. For precise investigations of the joining layer in the edge areas additional cross sections were prepared.

3.4 Results

In Fig. 8 selection of ultrasonic images of the test samples is shown. In samples with 25µm silver sinter layer thickness large fracture areas already after 500 temperature cycles are to be observed. By using Al instead of Cu base plates a small improvement regarding crack propagation is visible. It could be explained with the smaller young's modulus of the aluminum compared to

copper. Samples with 50µm and 100µm LTJ layer thickness only show small fracture areas even after 1500 temperature cycles. These cracked areas are significantly smaller than the observed cracks in large area solderings (see Fig. 2).

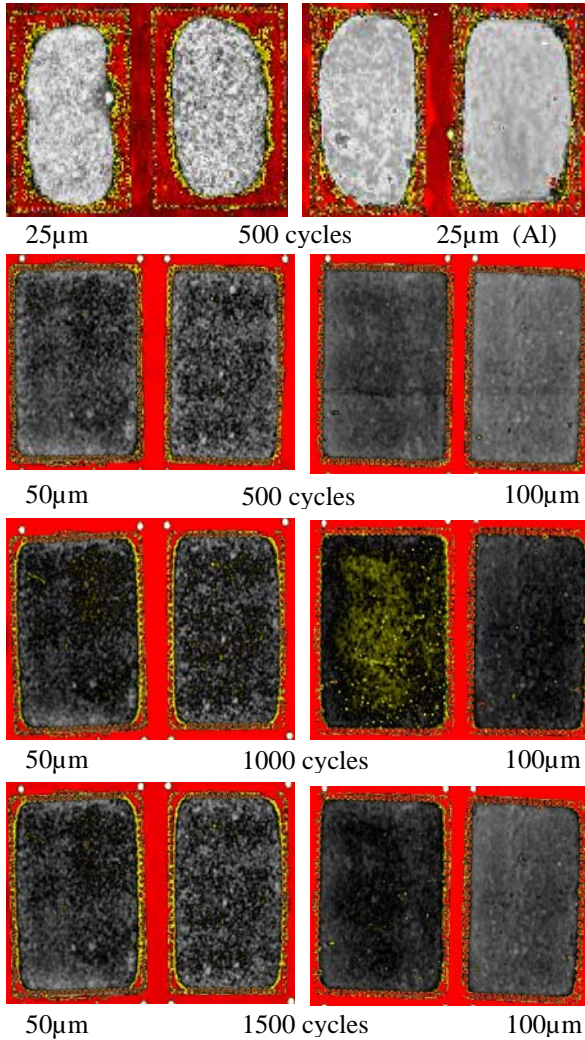


Fig. 8 Ultrasonic scans of the joining layers

This confirms the very good reliability of the test samples using LTJ technique. Due to the good results the test is continued in order to find the limits for the given DBC size and LTJ layer thicknesses.

Fig. 9 is showing the crack propagation of the test samples with 25µm layer thickness. The fracture path starts at the upper interfacial layer between Au metallization and sintered silver. This indicates low adhesion forces in this region. The crack propagates towards the middle of the LTJ-layer. It seems that for all samples the weak point is the joining layer outside dimple structure.

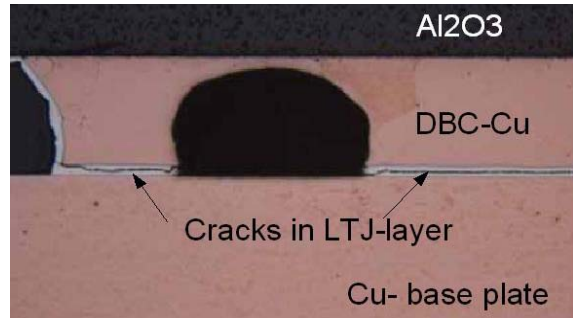


Fig. 9 Cross-section of the sample edge with about 25 µm LTJ-layer thickness

Samples with 50 and 100µm joining layer thickness indicate usually no further layer degradation behind dimple region. These samples have a long crack path in the interfacial layer between Au metallization and Ag sintered layer (see Fig. 10).

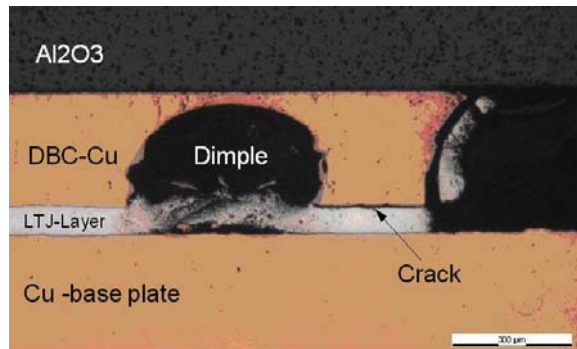


Fig. 10 Cross-section of the sample edge with about 50 µm LTJ-layer thickness

Crack lengths after 500 temperature cycles for samples with different layer thicknesses are shown in Fig. 11. A sintered silver layer should be thicker than 25µm to withstand the thermo-mechanical stress caused by a thermal cycling test (-40°C to +125°C).

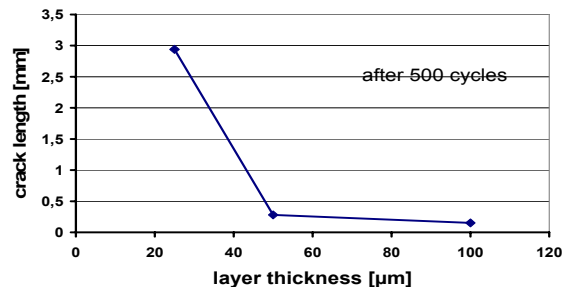


Fig. 11 Crack length after 500 cycles versus layer thickness.

The crack of a layer of 25µm is unexpected high compared to the lengths achieved with 50µm and 100µm of sintered silver.

To determine the crack propagation as a function of number of cycles all cracks of all DBC were measured in the corners (by omitting the dimple areas). The average crack length results are shown in Fig. 12 and lead to propagations speed of 0,3µm/cycle @ 100µm and 0,5µm/cycle @ 50µm. For soldered layers a propagation speed of 5µm/cycle for 100µm solder thickness is reported in [7]. The improvement is about a factor of ~10.

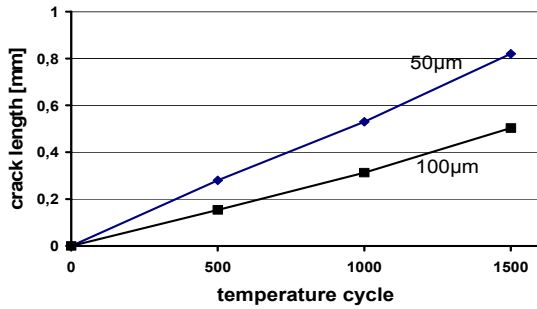


Fig. 12 Crack length propagation versus number of temperature cycles (-40°C to 125°C)

Tab. 4 Performance comparison

Performance Increase with LTJ-Substrate Bonding		
Type of substrate bond	No. of cycles*	ΔTjC [K]
200 µm solder layer	200	30,4
400 µm solder layer	350	32,5
100 µm sintered Ag layer	1500**	28,1
* failure condition: cracked area under die < 10%		
** test is continued		

The degradation of a LTJ-layer under temperature cycling conditions is significantly slower than in comparable solder joints. In Table 4 is shown that LTJ-Technique offers at least a factor 4 in lifetime and even a slight improvement of the ΔTjC of 4 K (~15%). The cost of the LTJ layer (100µm) is nearly equal to a thick solder layer of 400µm.

4 Outlook

In the near future further investigations are planned regarding different dimensions of the DBCs and thicknesses of the copper plate in order to improve the understanding of crack building principles. A second issue for future activities is the die assembly on a DBC as well as the DBC-on-heat sink assembly in a single step.

5 Summary

In this report is shown that LTJ-technique is capable of withstanding at least 1500 temperature cycles which is a factor of 10 higher compared to standard solder layers (100µm) and a factor of 4 higher compared to advanced process with 400µm. Together with published results about promising high number of power cycles [8] it now seems to be possible to manufacture high reliable power modules even for high ambient temperature conditions.

4 Literature

- Suppa, Manfred (Lackwerke Peters, Kempen): Die Anwendung druckbarer Heatsinks als Lösung von thermischen Problemen auf Leiterplatten. Referat 151, 8.FED Konferenz, 14.-16.9.2000 in Bayreuth
- Klaka, Sven (TU Braunschweig): Eine Niedertemperatur-Verbindungstechnik zum Aufbau von Leistungshalbleitermodulen, Cuvillier Verlag (1997)
- Poech, Max-Hermann (FhG-ISIT): Schädigungsmechanismen in Lötverbindungen bei erhöhter Temperatur. VTE 14 (2002) Heft 1, S. 12-18
- Poech, Max-Hermann (FhG-ISIT), Eisele, Ronald (Danfoss Silicon Power GmbH, Schleswig): Modelling the Mechanical Behaviour of Large-Area Solder Joints. PCIM conference proceedings (2000), Nuremberg
- Mertens, Christian (TU-Braunschweig): Die Niedertemperatur-Verbindungstechnik der Leistungselektronik. Fortschrittsberichte VDI, Reihe 21, Nr. 365 (2004)
- Rudzki, Jacek (TU-Braunschweig): Aufbaukonzepte für die Leistungselektronik mit der Niedertemperatur-Verbindungstechnik. Fortschrittsberichte VDI, Reihe 21, Nr. 376 (2006)
- Thoben, Markus: Zuverlässigkeit von großflächigen Verbindungen in der Leistungselektronik. Fortschrittsberichte VDI, Reihe 9, Nr. 363 (2002)
- Amro, R.; Lutz, J. (TU-Chemnitz); Rudzki, J. (FH-Kiel); Sittig, R. (TU Braunschweig); Thoben, M. (Infineon): Power Cycling at High Temperature Swings of Modules with Low Temperature Joining Technique. Conference proceedings ISPSD (2006), Naples, Italy