

# Sprayed Stress Reducing Interlayers for Highly Reliable Large Solder Joints

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## Abstract

The increasing demands in terms of reliability of power modules in automotive applications as well as in advanced industrial applications require new packaging solutions. An alternative to AISiC base plates is a base plate with a stress reducing interlayer. A way to deposit comparably thick interlayers is to spray powder of the desired materials to the base plates. In this paper the use of cold gas technology for the layer deposition will be discussed. It will be shown, how stress reducing interlayers increase the reliability of power modules.

## 1 Introduction

Power modules are subject to numerous temperature cycles during their life time. High temperature swings during power switching, or due to harsh environmental conditions, especially in automotive applications, leads to stress in the solder joints. Short power cycles result in wire bond lift off whereas long temperature cycles damage the solder joint between substrate and base plate. Addicted cracks in the solder joint increase the thermal resistance of the solder joint and thereby the temperature in the chip (junctions temperature). Again, this leads to wire bond lift off failures. These failure mechanisms are related to thermal and thermo-mechanical properties of the materials in the module. Today there are mainly two concepts to build up a power module.

### 1.1 Power Modules with and without Base Plate

Typically, power modules will be mounted on the heat sink using a thermal interface material (TIM). Either the DBC (Direct Bonded Copper) substrate or the base plate faces the heat sink (see fig. 1). This results in a different stack of materials, the so called thermal stack. Since the thermal conductivity of the TIM is relatively low, power modules can benefit from a base plate. The base plate provides a buffer function especially under dynamic load. Under static conditions the heat spreading effect in the base plates lead to a good thermal resistance

( $R_{th}$ ) between junction and heat sink. This is due to the fact, that the heat spreading effect helps to overcome the high thermal resistance of the TIM between module and heat sink. At modules without base plate, the contribution of the TIM to the  $R_{th}$  can reach up to 50% of the total  $R_{th}$ . However, the mismatch of the coefficient of thermal expansion (CTE) of the most important base plate material – copper – to the DBC substrate material is a lifetime limiting factor. The lifetime limit is given by the degradation of the solder between base plate and DBC [1].

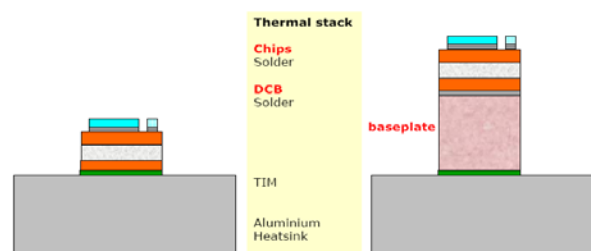


Fig.1 Modules with and without base plate

In the end the application dictates, which properties have to be achieved by the combined materials in a power module. Current material alternatives to copper base plates only provide sufficient thermo-mechanical properties in conjunction with insufficient thermal properties and higher cost. The target of this investigation is to maintain the benefits from copper base plates and to overcome the problems resulting from CTE mismatch.

## 1.2 Reliability Requirements

If the thermal stack requires a base plate for the reason of thermal improvements, it has to be cared for the matching of the thermo-mechanical properties. For high reliability applications, like automotive devices, modules are needed with a very good thermal stack and a very good stability against thermal cycling. To realise a sufficient cycle capability both joining partners (the base plates and the DBC) need a matching CTE. The target is to reduce the thermo-mechanical stress in the solder joint. The following diagram (fig. 2) shows the principle relationship between the expected life time and the difference of the CTEs of DBC and base plate ( $\Delta$  CTE).

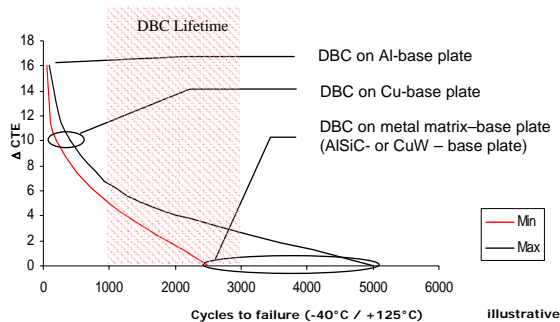


Fig. 2 Life time of modules with different base plates

The numbers of cycles to failure for higher values of the  $\Delta$  CTE are the result of different experiments. For lower values of the  $\Delta$  CTE the number of cycles to failure is a result of expectations with respect to the Coffin-Manson-relation. Resulting from the influence of soft solder material, solder thickness and different test conditions (e. g. dwell times, ...), the curves indicate a certain scatter band described by the Min and Max lines.

Perfect matching of substrates and base plates even leads to a failure mechanism caused by the non matching CTE of existing solder materials. This is the reason for the expectation, that even a  $\Delta$  CTE = 0 leads to a certain limit of the lifetime.

The lifetime limit for the modules may also be defined by the DBC itself. The lifetime expectancy of the DBC depends on the ceramic material ( $\text{Al}_2\text{O}_3$ ,  $\text{AlN}$ ,  $\text{Si}_3\text{N}_4$ , ... ) and the DBC process.

A thicker solder layer will help against solder cracks [2] but the thermal resistance is slightly increased. Furthermore, the thicker the solder layer, the higher the risk of tilting of DBCs during the soldering process.

## 1.3 Base Plate Technologies

Standard power modules with base plates use copper as heat spreader material. Cu has an excellent thermal conductivity (390 W/mK) but a high CTE (18 ppm/K) compared to the DBC (8 ppm/K). Due to this mismatch the thermo-mechanical shear forces in the solder joint will lead to cracks after a few hundred temperature cycles. Low CTE base plates like CuW or metal matrix structures as AlSiC will solve the problem with the thermal mismatch, but the total thermal resistance of the thermal stack will increase. The following table compares the relevant properties of different base plate materials (table 1).

Table 1: Properties of base plate materials

Technology	Thermal Resistance	Thermal Cycling capability	Cost
Cu base plate	++	-	+
Al base plate	-	--	++
AlSiC base plate	-	++	--
CuW base plate	0	++	--
stress reducing layer on Cu base plate	+	++	+

-- very negative characteristic - negative characteristic  
 0 neutral characteristic;  
 + positive characteristic ++ very positive characteristic

A new way to solve the problem with the thermal resistance vs. the thermal cycling capability is the introduction of a stress reducing interlayer on the base plate.

## 2 Base Plate with Stress Reducing Interlayers

### 2.1 The Principle of Stress Reducing Interlayers

The interlayer is designed to reduce the thermal mismatch between the DBC and the base plate. Therefore, the interlayer materials need a low CTE, in the range of the CTEs of the joining partners. Furthermore, in order to not adversely affect the thermal properties, a low thermal resistance of the interlayer material is required. Fig. 3 shows the schematic structure of a module with a stress reducing interlayer.

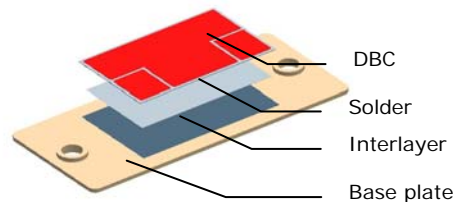


Fig. 3 Schematic structure of a module with a stress reducing interlayer

First it has to be defined, which material has to be applied, second the method of application has to be chosen.

### 2.1.1 Materials for the Interlayer

Table 2 shows the properties of some suitable materials for stress reducing interlayers. Those materials have a CTE in the typical range of materials that are used to build up power modules. Their thermal conductivity also is within a reasonable frame.

Table 2: Suitable materials for interlayers

Material	CTE [ppm/K]	Thermal Conductivity [W/mK]
Nickel	13,3	90
Copper	17	400
Molybdenum	5	146
Tungsten	4,5	200
AlSiC	7 - 14	150 - 200
Tungsten/Copper 60 W / 40 Cu [wt.%]	12,1	270
Tungsten/Copper 80 W / 20 Cu [wt.%]	8,3	200
Molybdenum/Copper 80 Mo / 20Cu [wt.%]	7,2	160

The choice of the material for the interlayer will also be affected by availability and cost.

In order to achieve layer properties, comparable to the bulk material properties, given in table 2, the porosity of the layer shall be low.

Furthermore, a solderable surface is required to be able to apply the standard module manufacturing processes (i. e. soldering of the DBC).

Of course the joint between the base plate and the interlayer itself should be mechanically strong and should not lead to additional thermal resistance.

### 2.1.2 How to Apply the Interlayers

There is quite a variety of classical methods to apply interlayer material to the base plates:

- Adhesive bonding
- Soldering
- Plating

Adhesive bonding processes are well known but lead to very bad thermal resistance due to the additional adhesive layer.

Also soldering will result in an additional layer between base plate and interlayer. Again, the to-

tal thermal resistance would be increased. In order to enable a second soldering step, solder with a high melting point might be required. Those solder materials are lead based or are very expensive like AuSn.

In general, plating processes like galvanic or chemical deposition or sputtering only allow to build up very thin layers. However, thicker layers are required for the compensation of CTE mismatch.

To get thick layers a more efficient method for the deposition of materials is required. Different methods of spraying powders lead to layer thicknesses in the order of millimetres (e.g. flame spray, plasma spray, ...).

An appropriate method of spraying powder is the comparably new cold gas technology.

## 2.2 Cold Gas Technology

Cold gas technology is not based upon melting the powder by thermal energy. Instead, the particles are welded to the surface using their kinetic energy when hitting the surface at a very high velocity (about 300 – 900 m/s). In one step, the powder particles are applied to the substrate and in the same time are forming a joint with their target. Figure 4 shows the principle of the technology.

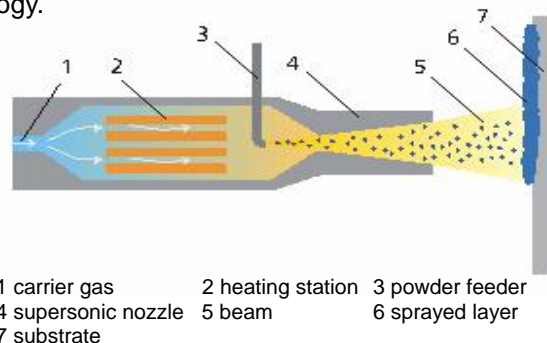


Fig. 4 Principle of cold gas technology (sketch by courtesy of CGT, Germany)

The main advantages of this technology are:

- low oxide content
- high thermal and electrical conductivity (very close to bulk material properties)
- minimal heat affection of the substrate
- high density
- minimal grain growth
- high coating efficiency

Figure 5 shows typical cold gas equipment with the control unit, the heater with the powder feeder and the spraying gun. Not shown is the optional robot to move the spraying gun, the cabin to shield the environment from the process and the stencil to exactly define the target area.



Fig. 5 Components for cold spray technology (by courtesy of CGT, Germany)

To define the geometry of the interlayer a stencil is used with an opening for the area to be coated. By moving the spraying gun in parallel lines over the substrate using a robot the powder is sprayed onto the unprotected areas of the base plate. The thickness of the interlayer will be adjusted by the speed of the robot and by the number of spraying cycles. With cold gas technology it is comparably easy to create thick layers of different materials onto base plates. It is also possible to spray "alloy-like" mixtures of different powders to achieve tailored interlayer properties [3].

### 2.3 Simulation of the Resulting CTE of Base Plate and Interlayer

Simulations of a sprayed interlayer on a base plate should indicate the effect of the resulting CTE on the surface. For the simulation a thin layer of the plating material is added to the top of a copper plate. At the reference temperature the sandwich is at equilibrium state and is then heated up. The resulting deformation, due to the differences of the CTE, is calculated and translated into a CTE resulting at the surface of the interlayer (see Fig. 6).

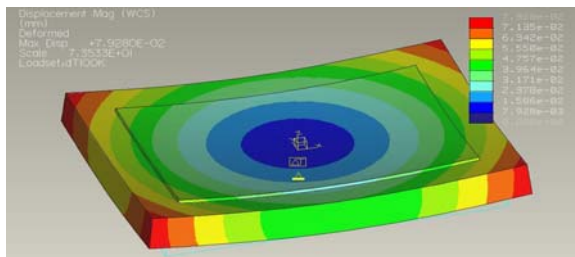


Fig. 6 Thermo-mechanical simulations

In this example the layer measures 42mm x 29,2mm. The copper base plate is 52mm x 39,2mm (i.e. 10mm larger in the x, y directions than the layer). The thickness of the base plate is 3mm whereas the CTE layer thickness is varied from 100 $\mu$ m to 1mm. The resulting CTE depending on the thickness of the interlayer is shown in figure 7 for different materials.

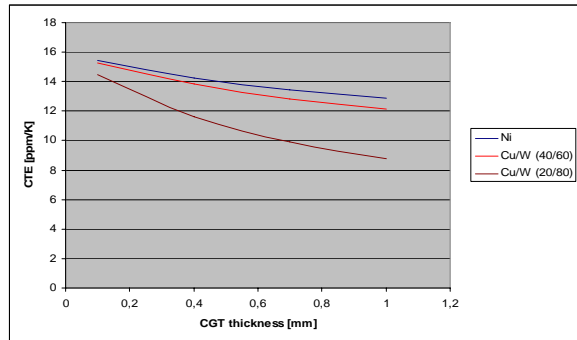


Fig. 7 Resulting CTE depending on the layer thickness for different materials

The resulting thermal resistance of the base plate with interlayer is calculated for different materials and layer thicknesses. The results are shown in figure 8.

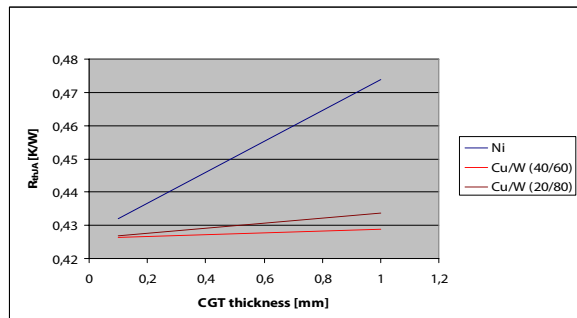


Fig. 8 Resulting  $R_{th}$  depending on CGT thickness

To verify the results of the simulation, a measurement with a strain gauge shows a resulting CTE of 15ppm/K on a 500 $\mu$ m thick Ni interlayer on a 3mm thick Cu base plate. This is well within the expectations from the simulation results.

### 2.4 Experiments

For the first demonstrators (see fig. 9) nickel was used as material for the interlayer. The CTE of pure Ni is 13ppm/K. This is in-between the CTE of a DBC (8ppm/K) and the Cu base plate (18ppm/K). Furthermore, Ni powder was available at the time, the demonstrators have been produced.



Fig. 9 Demonstrator with a 500µm Ni layer  
The nickel layer has an area of 47mm to 26mm and a thickness of 500µm and 1000µm. On this sprayed Ni layer the DBC was mounted (42mm to 25mm) in a vacuum soldering process with SnAg3.5 solder. An X-ray analysis (see fig. 10) reveals a few small voids in the solder joint. This is mainly due to the fact, that the solder process parameters have not yet been optimized.

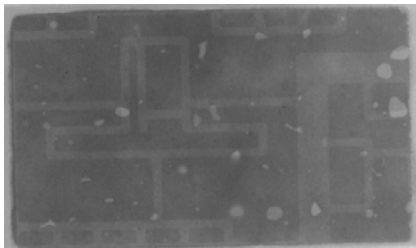


Fig. 10 X-ray analysis of the solder joint

With optimized soldering parameters the voids can be eliminated. A cross-section (see fig. 11) shows a good wetting of the solder on the sprayed Ni layer.

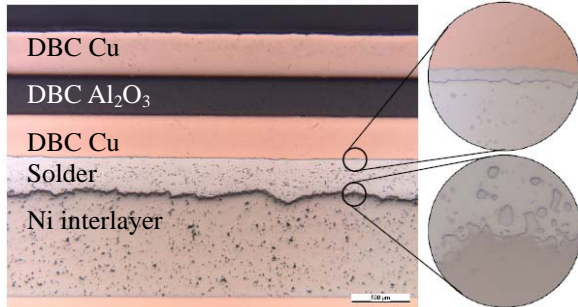


Fig. 11 Cross-section of a solder joint with a sprayed Ni layer

For reliability tests the demonstrators with the sprayed Ni interlayer were stressed with fast temperature cycles (-40°C ... +125°C) with a dwell time of 30min (according to [4]). After defined temperature cycles the demonstrators were inspected using scanning acoustic microscopy.

Ultrasonic scans (see Fig. 12) show first cracks in the solder layer between 1000 and 1500 temperature cycles.

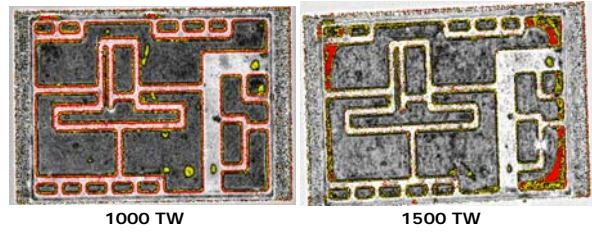


Fig.12 Cracks in the solder layer

If the cracks reach the area under a semiconductor the thermal resistance increases and the chip will heat up and fail because the wire bonds will lift off. Large area solder joints without stress reducing interlayer will usually fail at 100 to 300 temperature cycles. Among other boundary conditions, the exact number of cycles to failure depends on the size of the solder area, the solder thickness and the solder material.

The joint between sprayed layer and base plate does not show any cracks in the interface after 1500 temperature cycles which is presented in the following ultrasonic scans (see Fig. 13).

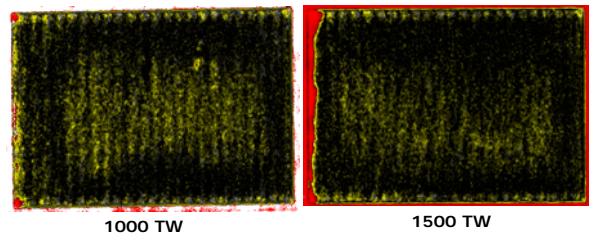


Fig.13 Ultrasonic scan of the interface between interlayer and base plate

A cross-section analysis confirms the results of the scanning acoustic microscopy.

These results fit in the curves shown in figure 2 (see fig. 14, respectively). The  $\Delta$  CTE between base plate with stress reducing Ni interlayer and DBC is around 5ppm/K. The number of temperature cycles to failure is 1000 ... 1500. This is well within the expectations discussed in chapter 1.2.

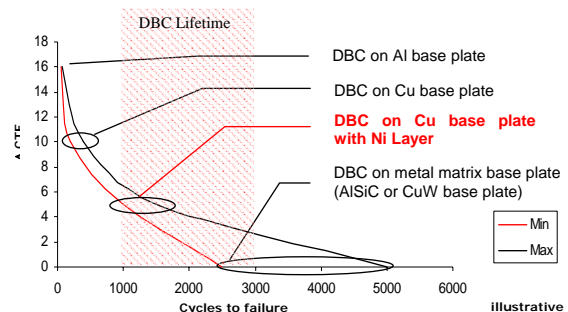


Fig. 14 Life time of sprayed Ni layers

### 3 Outlook on Currently Running Experiments

To further reduce the  $\Delta$  CTE between base plate and DBC new spraying powders are necessary. New materials still need to have a low CTE and good thermal conductivity (see table 2). "Alloy-like" mixtures like Copper/Tungsten will reach the desired properties. First experiments show that it is possible to spray a mix of two different powders. Figure 15 shows such a Cu/W layer on a Cu base plate.

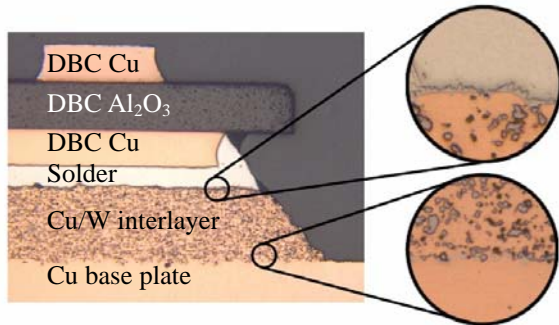


Fig. 15 Cross section of a solder joint with a Cu/W layer

Today it is possible to spray Cu/W powder with a ratio of 40/60 [wt.%]. The correlation between metal ratio (Cu/W) and the properties of the layer is shown in figure 16.

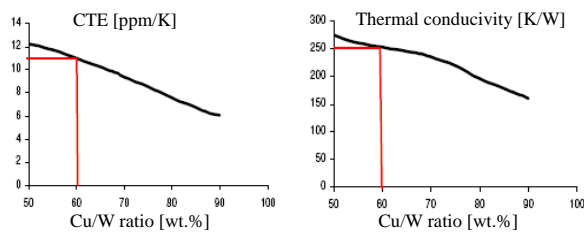


Fig. 14 correlation between Cu/W ratio and material properties

A Cu/W powder with a ratio of 20/80 [wt.%] and a high spray efficiency factor currently is under development. It is expected, that interlayers made from Cu/W 20/80 [wt.%] will result in a  $\Delta$  CTE near zero so that highest stability in temperature cycles can be achieved.

The limiting factor still is the solder material itself. If the solder material could be substituted by a material with a higher melting point (leading to higher stress resistance) the lifetime expectations could be even higher. This would lead to completely new processes for bonding and joining. One of the most promising techniques is the "Low temperature joining" process (LTJ).

### 4 Conclusion

The correlation between power module lifetime and  $\Delta$  CTE is the Coffin-Manson relation. Expectations for the effect of a low  $\Delta$  CTE have been proved to be true by simulations and experiments. It could be shown, that solder joints on stress reducing interlayers have a longer lifetime expectancy than those on uncoated copper base plates.

The process of cold gas technology has been chosen to apply suitable interlayer materials in a suitable thickness in order to be fully compatible with the standard power module manufacturing processes.

The lifetime of large area solder joints between base plates and substrates of power modules could be extended by a factor of more than 10.

Furthermore the thermal properties of Cu base plates with stress reducing interlayers are better compared to AlSiC base plates.

It can be concluded, that sprayed stress reducing interlayers could be a cost effective alternative to metal matrix base plates (e. g. AlSiC or CuW).

### 5 Literature

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